Short Papers

The Frequency-Dependent Impedance of p-i-n Diodes

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Abstract — **The purpose of this paper is to demonstrate that the impedance of the p-i-n diode is definable as a function of frequency and depends on the diode's geometry and electronic properties. A procedure for calculating the equivalent series p-i-n diode impedance is presented and compared with experimental resistance versus frequency data for silicon p-i-n diodes. A procedure is also outlined for determining diode parameters for a desired resistance–frequency response.**

I. Introduction

The impedance of a forward-biased p-i-n diode is a primary electrical parameter that determines performance in phase shifters, switches, and attenuator circuits. Frequently, however, the frequency of the application is often substantially different, either higher in the microwave range or lower in the RF range, from the manufacturer's test frequency (generally between 100 MHz and 1 GHz). When first introduced, the p-i-n diode was used in VHF and microwave frequency applications, but there has been significant development in recent years of circuits containing p-i-n diodes at frequencies extending below 1 MHz [1], [2]. In analyzing circuits containing p-i-n diodes, a common assumption used is that the total p-i-n diode impedance is controlled by the charge stored in the i-region by the ac and dc currents (I_k and I_0, respectively). At high frequencies, this assumption is valid, and was discussed in Leenov's paper [3]. At low frequencies, the p-i-n diode's distortion properties have been found to be a function of this time-varying stored charge [4]–[6]. In addition to these nonlinearities, resistive and reactive effects are introduced by the semiconductor junctions that may be significant enough to dominate the overall device impedance. Earlier theoretical work has indicated that the junction effects are sensitive to device parameters such as i-region carrier lifetime (τ) and i-region thickness (W) [7]–[9], and constitute a substantial component of the overall device impedance. In these papers, however, only a small amount of experimental data was presented. Garver [10] presents a p-i-n diode model to include these junction effects, but does not consider the reactive effects of the i-region conductivity modulation. The effects of the junctions on the p-i-n diode's low-frequency characteristics have received some attention more recently [11], but only the resistive effects were discussed.

This paper will demonstrate that the total p-i-n diode impedance becomes virtually a constant resistance above a specific frequency, but at low frequencies, a significant capacitive or inductive component may be present. Analysis of the frequency-dependent impedance is especially important in short-lifetime p-i-n diodes [11], [12], where the so-called low-frequency effects may actually extend to several hundred MHz. The material presented in this paper shows the basis for calculating the small-signal impedance of the p-i-n diode from its dc value (the slope of the current–voltage characteristic) to its value at microwave frequencies. Experimental data are presented on the forward-biased resistance and reactance of silicon p-i-n diodes of various geometries that verify the analysis. The model is applicable to packaged, beam lead, and chip p-i-n diodes fabricated from silicon and gallium arsenide; package and substrate parasitic impedances are neglected.

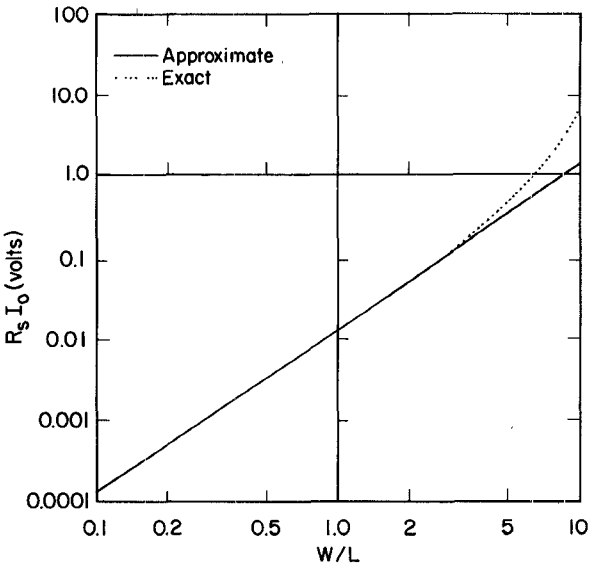

Fig. 1. Graph of the i-region resistance–bias current product versus the diode geometry ratio W/L. For values of W/L greater than approximately 2.5, eq. (1) underestimates the resistance; therefore, the more exact relationship (eq. 2) should be used.

II. Analysis

The traditional high-frequency p-i-n diode resistance expression, R_I, is given by [13]

$$R_I = W^2/2\mu Q = (W/L)^2 V_T/2I_0 \qquad (1)$$

where $V_T = kT/q$, μ is the ambipolar mobility, L (the diffusion length) $= (D\tau)^{1/2}$, D is the ambipolar diffusion constant, and Q ($= I_0\tau$) is the i-region stored charge. Equation (1) applies to thin i-region p-i-n diodes where $W/2L$ is less than unity, and at frequencies well above $1/\tau$. The more exact equation that applies to all p-i-n diodes can be derived by integrating the injected charge density in the i-region over the entire i-region length (Fig. 1); namely

$$R_I = \int_0^{W/2} dx/Aq\mu n_0(x)$$
$$= 4V_T \sinh(W/2L)\left[\tan^{-1}(e^{W/2L}) - \pi/4\right]/I_0 \qquad (2)$$

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where

$$n_0(x) = I_0 L \cosh(x/L)/2AqD \sinh(W/L)$$

and A is the i-region area. Equation (2) reduces to (1) if the ratio $W/2L$ is less than unity. Both equations apply only to the i-region resistance and are high-frequency equations, implying that all effects of the junctions (a low-frequency phenomenon) are neglected. Fig. 1 shows a plot of the resistance–bias current product $R_I I_0$ versus the ratio W/L, computed using (1) and (2). Note that for values of W/L greater than approximately 2.5, (1) underestimates the $R_I I_0$ product; hence, (2) should be used for estimating the resistance of these diodes.

At dc, the total p-i-n diode impedance is the dynamic resistance of the junctions, namely, $2V_T/I_0$, and may be derived from the dc diode characteristics observed on a curve tracer. At low frequencies, both the NI and the IP junctions (which can individually be modeled as an impedance, Z_J) cause reactive effects associated with diffusion of carriers across the junction. In the intrinsic region, reactive effects caused by conductivity modulation also contribute significantly to the total p-i-n diode impedance, Z_T, such that Z_I may be only a small part of Z_T in the low-frequency limit. The total p-i-n diode impedance as a function of frequency may then be written as

$$Z_T(f) = Z_I(f) + 2Z_J(f). \tag{3}$$

The factor of 2 in (3) appears because of the two junctions in the ideal p-i-n diode.

Expressions for Z_J and Z_I have been derived by applying the basic semiconductor equations [14] to obtain the junction and the i-region voltages [11], [15] as a function of the ac and dc current levels. The ac component of the junction voltage may be written as

$$V_j(t) = V_T \ln\left[1 + \mathrm{Re}\left\{ n_1(W/2) \exp(j\omega t)/n_0(W/2)\right\}\right] \tag{4}$$

and the ac component of the i-region voltage may be written as

$$V_i(t) = \frac{I_0 + I_1 e^{j\omega t}}{Aq\mu} \int_0^{W/2} \frac{dx}{n_0(x)\left[1 + \mathrm{Re}\left\{ \dfrac{n_1(x)}{n_0(x)} \exp(j\omega t)\right\}\right]} \tag{5}$$

where

$$n_1(x) = \frac{I_1 L}{2AqD} \frac{\cosh\left[x(1+j\omega\tau)^{1/2}/L\right]}{\sinh\left[W(1+j\omega\tau)^{1/2}/2L\right]} (1+j\omega\tau)^{-1/2}$$

and ω is the angular frequency. By using a small-signal assumption (I_k/I_0 less than unity), (4) and (5) are used in deriving the individual p-i-n diode impedance components ($Z_J = V_j/I_1$ and $Z_I = V_i/I_1$) at any frequency. The details of this derivation will be presented in a future paper.

The results of this analysis show that at frequencies substantially greater than $1/\tau$ (approximately $10/\tau$), the resistance approaches the value predicted by (1) and (2). At frequencies below $10/\tau$, however, the impedance versus frequency behavior is strongly dependent on device geometry and lifetime. The reactance of the device may be inductive or capacitive at low frequencies, as will be shown in the next section.

III. Experimental Results

The model was applied in investigating the impedance versus frequency for p-i-n diodes with different i-region thicknesses and lifetimes. Impedance measurements were performed using the HP-4192A LF Impedance Analyzer. A dc forward bias was applied through the analyzer, and the RF current was kept less than the dc bias current. The silicon p-i-n diodes tested were packaged in axial lead glass diode packages.

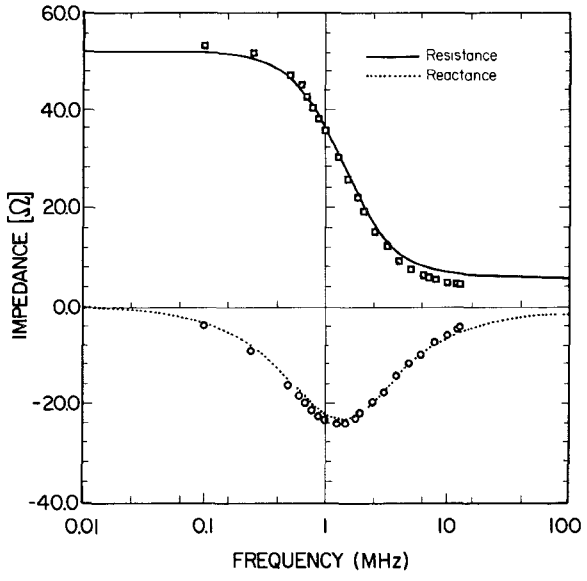

Fig. 2. Graph comparing the calculated and measured resistance and reactance values of a silicon p-i-n diode at a dc bias current of 1 mA (W = 0.42 mils, Q = 116 pC).

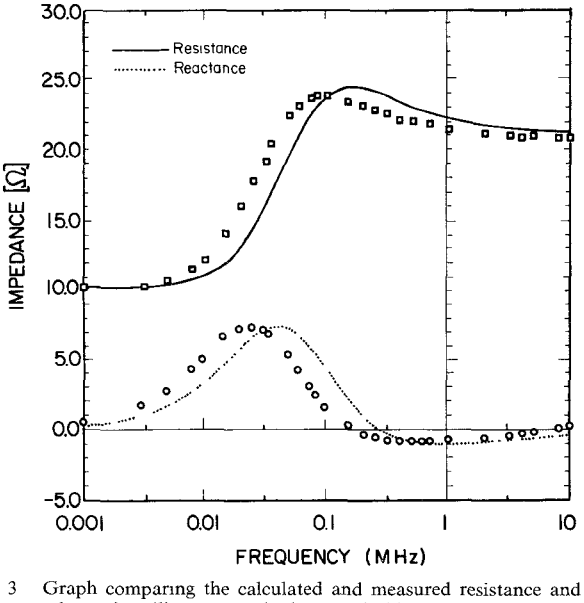

Fig. 3. Graph comparing the calculated and measured resistance and reactance values of a silicon p-i-n diode at a dc bias current of 5 mA (W = 10.8 mils, Q = 19 nC).

Carrier lifetime was derived from diode stored charge at fixed forward bias currents. The instruments used to measure stored charge (Bermar Corp. models 63 and 83 stored charge meters) essentially measure the area of the reverse recovery current trace ($Q = \int i\,dt$). Stored charge as the basis for carrier lifetime is also better applicable to p-i-n diode impedance analysis than reverse recovery time since it directly relates to i-region conductivity modulation.

Figs. 2 and 3 show computed resistance and reactance plotted versus frequency with experimental data on silicon p-i-n diodes of different physical and electrical characteristics. Fig. 2 presents

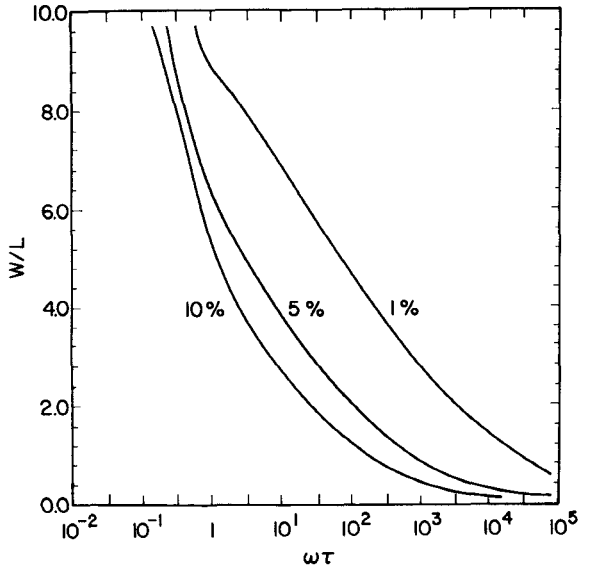

Fig. 4. Graph of the ratio W/L versus the angular frequency–carrier lifetime product for three different variations in p-i-n diode resistance: 10 percent, 5 percent, and 1 percent.

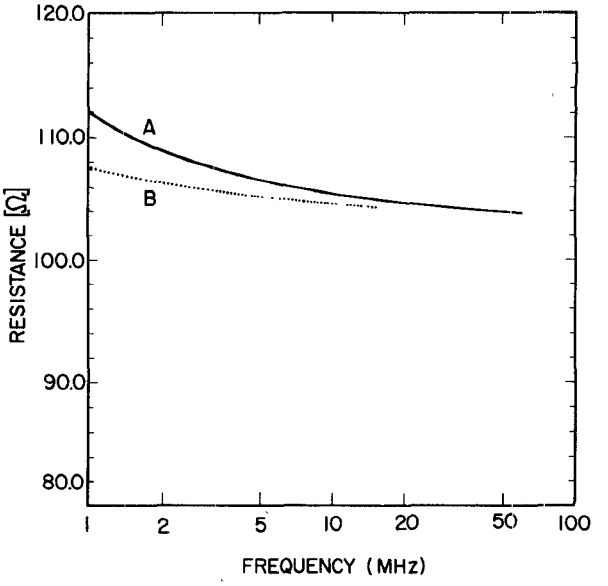

Fig. 5 Graph of the resistance–frequency response for two p-i-n diodes Curve A: $\tau = 2.54$ μs, $W = 8.8$ mils; Curve B: $\tau = 10$ μs, $W = 17.5$ mils Note that the thicker p-i-n diode (curve B) gives the flatter resistance–frequency response.

results for a thin-i-region, short-lifetime diode ($W = 0.42$ mils, $\tau = 116$ ns). Note the transition region in the 1 to 10 MHz range where the impedance changes dramatically, indicating the region where the impedance changes from being dominated by the junctions to being dominated by i-region effects. There is good agreement between the model and the experimental data.

Fig. 3 compares the model with measurements on a thicker, longer lifetime silicon p-i-n diode ($W = 10.8$ mils, $\tau = 3.8$ μs). The low-frequency reactance is inductive in nature, as predicted by the model, and remains inductive up to approximately 200 kHz. At higher frequencies, the reactance becomes capacitive and completely disappears at high frequencies. The data show good agreement with the model computations.

IV. Application Example

The p-i-n diode finds frequent use in such gain control applications as signal generator leveling circuits. In these applications, it is desirable to have the p-i-n diode resistance at a fixed applied dc current constant over a wide frequency range. The analysis has focused on the prediction of the frequency-dependent impedance of the p-i-n diode using the parameters W and $\omega\tau$. This information makes it possible to design values for W and τ that minimize the variation of resistance with frequency. Fig. 4 shows a plot of W/L versus $\omega\tau$, indicating the values of W/L and $\omega\tau$ where the total diode resistance is within 10 percent, 5 percent, or 1 percent of its high-frequency value computed using (3). The use of these curves in determining optimum W and τ values may be illustrated by the following example. Suppose that an application requires that the p-i-n diode resistance not change more than 10 percent from 100 Ω (at 1 mA) from microwave frequencies to 1 MHz. The required value of W/L may be found from Fig. 1 to be approximately 2.75 ($R_s I_0 = 0.1$ V). Fig. 4 shows that for a 10 percent variation in diode resistance at $W/L = 2.75$, a minimum value of $\omega\tau = 16$ must be used. The minimum required i-region carrier lifetime may then be computed as

$$\tau = \omega\tau/2\pi f = 2.54\ \mu\text{s}. \tag{6}$$

The minimum i-region thickness W (at the minimum computed lifetime) may then be derived using

$$W = [\mu V_T \tau]^{1/2}(W/L) = 223\ \mu\text{m} = 8.8\ \text{mils}. \tag{7}$$

Thus, an 8.8 mil p-i-n diode with a 2.5 μs i-region carrier lifetime will show less than a 10 percent variation in resistance above 1 MHz. Fig. 5 shows the resulting resistance–frequency response of this p-i-n diode. Also shown in Fig. 5 (curve B) is the resistance–frequency response of a device with a 10 μs i-region carrier lifetime (which is above the minimum lifetime required in this example) and a corresponding i-region thickness of 440 μm (17.5 mils). Note that for frequencies above 1 MHz, the thicker p-i-n diode shows a flatter resistance–frequency response.

V. Conclusions

A generalized model of a forward-biased p-i-n diode showing its impedance dependence with frequency has been presented and verified with experimental data. The model predicts that at frequencies much higher than $1/\tau$, the total resistance decreases to its i-region resistance limit. At lower frequencies, however, the resistance behavior with frequency is complex and a function of the diode geometry and carrier lifetime. The model also indicates that p-i-n diodes with thicker i-region widths have less change in resistance at frequencies higher than $1/\tau$ than do thinner diodes for the same carrier lifetime. The reactance of the p-i-n diode as derived from the model indicates that at frequencies much higher than $1/\tau$, the reactance is very small and is virtually negligible. Many p-i-n diodes are used at microwave frequencies but are specified for forward resistance at a lower frequency (generally between 100 MHz and 500 MHz). For p-i-n diodes used as switch elements the lower frequency value will give a pessimistic result if used to calculate circuit loss. For applications at frequencies lower than the test frequency and for attenuator applications, the resistance should be computed from the p-i-n diode characteristic.

REFERENCES

[1] P Basile et al. "Solid state antenna switching," *RCA Rev*, vol 42, p. 752. Dec. 1981.
[2] M. Caulton, A Rosen, P. Stabile, and A. Gombar, "p-i-n diodes for low frequency high-power switching applications," *IEEE Trans Microwave Theory Tech.*, vol. MTT-30, p. 875, June 1982.
[3] D Leenov, "The silicon PIN diode as a microwave radar protector at megawatt levels," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 53–61, Feb. 1964.
[4] R. Caverly and G Hiller, "Distortion in p-i-n diode control circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, p. 492, May 1987.
[5] G. Hiller and R. Caverly, "Predict PIN-diode switch distortion," *Microwaves and RF*, vol. 25, p. 111, Jan 1986.
[6] R. Caverly, "A nonlinear p-i-n diode model for use in multi-diode microwave and RF communication circuit simulation," in *Proc. 1988 IEEE Int. Symp Circuits Syst.*, June 1988, pp. 2295–2299.
[7] J. Nordman and R. Greiner, "The small-signal inductive effect in a long PIN diode," *IEEE Trans. Electron Devices*, vol. ED-10, p. 171, 1963.
[8] N. Prima and Y. Tkhorik, "Total impedance of a p-i-n diode a high injection levels," *Sov. Phys.—Semicond.*, vol. 1, no. 4, p. 444, Oct. 1967.
[9] R. Varshney, D. Roulston, and S Chamberlain, "Some properties concerning the a.c. impedance of P-I-N and P-N-N^+ diodes," *Solid-State Electron.*, vol. 17, p. 699, 1974.
[10] R. Garver, *Microwave Diode Control Devices*. Dedham, MA: Artech House, 1976, pp. 326–329.
[11] R. Caverly and G. Hiller, "Microwave resistance of gallium arsenide and silicon p-i-n diodes," in *1987 IEEE MTT-S Int Microwave Symp. Dig.*, p. 591.
[12] C. Barratt *et al* "New GaAs PIN diodes with lower dissipation loss, faster switching speed at lower drive power," in *1983 IEEE MTT-S Int Microwave Symp Dig*, p 507.
[13] J. White, *Semiconductor Control*. Dedham, MA: Artech House, 1977.
[14] S M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.
[15] W. Reiss, "Volterra series representation of a forward biased p-i-n diode," *IEEE Trans. Electron Devices*, vol. ED-28, p. 1495, Dec 1981

Development and Evaluation of a GaAs MMIC Phase-Locked Loop Chip Set for Space Applications

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***Abstract*—GaAs monolithic microwave integrated circuit (MMIC) chips designed for a phase-locked loop frequency source to be used in space applications have been developed. The chip set includes a three-stage resistive feedback amplifier (RFA) with 13 dB gain in a 275 MHz to 5.85 GHz bandwidth, a 2.0 GHz voltage-controlled oscillator (VCO), a 2.8 GHz digital prescaler, and a VHF/UHF digital phase/frequency discriminator. Both analog and buffered-FET logic (BFL) digital circuits were fabricated on the same wafer. The MMIC process which was developed for this application comprises molecular beam epitaxial (MBE) deposition of the active layer, proton isolation, submicron gates, thin-film TaN resistor deposition, and silicon nitride passivation. The chip set was used successfully to implement a 2.0 GHz all-GaAs phase-locked loop (PLL).**

I. INTRODUCTION

MMIC's will have a major impact on communication satellite payloads of the future. One area of direct application is in fixed-frequency local oscillators (LO's) which are used for frequency mixing circuits throughout modern payloads. Conventional hybrid LO's are both bulky and heavy, making them highly unsuitable for phased array antenna applications.

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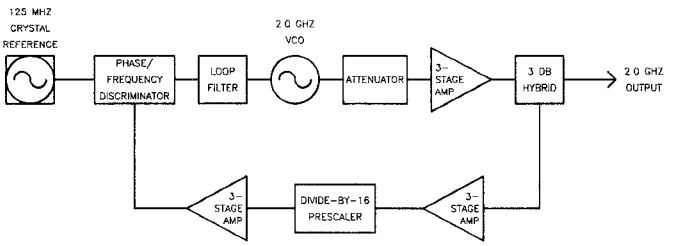

Fig. 1 GaAs MMIC phase-locked loop block diagram

Development of a generic GaAs PLL chip would greatly reduce the weight, size, and cost of an LO reference source while providing inherent radiation hardness. The stabilization of a microwave frequency source and the reduction of off-carrier noise density by means of a crystal oscillator and PLL have been described by Ohira *et al.* [1]. Additionally, MMIC chips suitable for use in PLL's have been reported [2]–[5]. In this paper, the implementation of MMIC's in a GaAs PLL integrated on a single breadboard is described. The basic analog and digital building blocks (the RFA, prescaler, VCO, and phase/frequency discriminator) have been fabricated monolithically on a single GaAs wafer and assembled into a MMIC PLL. The PLL design approach, processing technology, individual chip results, loop integration, and noise reduction will be discussed.

II. PHASE-LOCKED LOOP DESIGN

The primary goal of this project was to develop a 2.0 GHz MMIC PLL chip for use as an LO in satellite payloads. By designing a PLL with a wide capture range, a generic LO chip could be used in different satellite applications whereby the mere selection of a crystal reference would determine the LO frequency. Fig. 1 shows a block diagram of the MMIC/MIC phase-locked loop developed to this point. The PLL is a classical second-order design having passive *RC* loop filtering. The PLL has a 125 MHz crystal reference source that feeds the digital phase/frequency discriminator. A 2.0 GHz common-gate VCO provides the PLL microwave signal, while resistive-feedback amplifiers (RFA's) supply gain where needed in the loop. A prescaler scales the 2.0 GHz signal for feedback into the phase/frequency discriminator.

III. PROCESS DESCRIPTION

The process developed for the fabrication of the chips described in this paper comprises the following features:

- molecular beam epitaxial (MBE) deposition of the active layer,
- isolation of the active regions by proton-induced damage,
- thin-film tantalum nitride resistors,
- 0.75-μm-gate FET's,
- Schottky level-shifting diodes,
- metal–insulator–metal (MIM) capacitors with silicon nitride dielectric,
- air bridge second level interconnections (Fig. 2),
- silicon nitride passivation.

The MBE material, deposited sequentially on an undoped semi-insulating substrate, consists of a 0.4-μm-thick undoped